Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **OUTPUT A**
2. **INPUT A-**
3. **INPUT A+**
4. **V-**
5. **INPUT B+**
6. **INPUT B-**
7. **OUTPUT B**
8. **V+**

**.042”**

**.064”**

**7**

**8**

**1**

**6 5**

**4**

**2 3**

**MASK**

**REF**

**Y**

**1**

**5**

**5**

**8**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: V-**

**Mask Ref: Y**

**APPROVED BY: DK DIE SIZE .042” X .064” DATE: 7/7/22**

**MFG: NATIONAL THICKNESS .015” P/N: LM1558**

**DG 10.1.2**

#### Rev B, 7/1